R18

Code No: 153AB

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD B.Tech II Year I Semester Examinations, March - 2021 ANALOG AND DIGITAL ELECTRONICS

(Common to CSE, IT, ITE)

Time: 3 hours Max. Marks: 75

Answer any five questions All questions carry equal marks

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- 1.a) Derive the expression for ripple for the circuit FWR with inductor filter.
 - b) Explain the working of semiconductor photo diode.

[8+7]

[7+8]

- 2.a) Explain V-I characteristics of a tunnel diode and write its applications.
 - b) Define clipping and clamping circuits. Differentiate clipping and clamping circuits. [7+8]
- 3.a) Draw the circuit diagram of an NPN junction transistor in CE configuration and describe its characteristics.
 - b) For the transistor amplifier circuit, when signal changes by 0.012 V, the base current changes by 9 μA and collector current by 1.3 mA. If the collector load $R_C = 6 \ K\Omega$, $R_L = 12 \ K\Omega$. Determine input resistance, current gain and voltage gain. [9+6]
- 4.a) What is the necessity of biasing circuits? Derive the expression for stability factor of self-bias circuit.
 - b) Derive the expressions for Zi, Zo and Av for common drain J-FET amplifier. [8+7]
- 5.a) Draw a totem-pole output buffer with a TTL gate. Explain its operation.
 - b) Draw the circuit of artimproved version of D.T.L. 3-input NAND gate, and explain its operations with the delp of Truth Table. If h FE of each transistor is 40, find FAN-OUT of the circuit. [8+7]
- 6.a) Simplify the following function using K-map. $F(A,B,C,D) = \Sigma(1,3,4,5,6,11,13,14,15)$
 - b) Draw the logic circuit of a 3 to 8 decoder and explain its working.
- 7.a) Design a 4-bit comparator circuit using logic gates.
 - b) Design a modulo 10 counter using JK flipflops and explain its timing diagram. [7+8]
- 8.a) Using D-Flip flops and waveforms, explain the working of a 4-bit SISO shift register.
 - b) Difference between static and dynamic RAM. Draw the circuits of one cell of each and explain its working. [7+8]

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